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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
AUDUONG, GENE NGHIA

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 05/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/090,902	Applicant(s) LEE ET AL.	
	Examiner Gene N Auduong	Art Unit 2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-16 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-16 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Objections

2. Claim 6 is objected to because of the following informalities: the limitation: second electrical signal is the second impurity region (drain voltage) as stated in the independent claim 1. How can the second signal (drain voltage) is substantially equal to the second and first voltage as claimed? Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Ono et al. (U.S. Pat. No. 4,884,239).

Regarding claim 1, Ono et al. disclose a method for performing an erase operation in a non-volatile memory device comprising a bulk region of a first conductive type (p-type substrate), spaced first and second impurity diffusion regions of a second conductive type formed in the bulk region (n-type impurity regions formed in the substrate region), a charge storing layer formed between the first and the second impurity diffusion regions (see figures 5-6), and a conductive electrode formed on the charge storing layer, the method comprising the

steps of: applying a bulk voltage to the bulk region for a predetermined erase time (0 V is being applying to the substrate at node VB); applying a gate voltage to the conductive electrode for the predetermined erase time (applying a gate voltage Vg to the control gate 47), the gate voltage being greater than **or equal** to the bulk voltage (Vg = VB = 0 volt); applying a first electrical signal to the first impurity diffusion region for the predetermined erase time (applying source voltage Vs to the source region), the first electrical signal comprising a voltage that is greater than the gate voltage (Vs = 2 volts > Vg = 0 volt); and applying a second electrical signal to the second impurity diffusion region for the predetermined erase time (applying drain voltage Vd to the drain region), the second electrical signal comprising a voltage that is greater than the gate voltage (Vd = 14 volts > Vg = 0 volt), wherein the voltage of the first electrical signal is different from the voltage of the second electrical signal (Vd = 14 volts not equal to Vs = 2 volts; also see col. 5, lines 14+).

Regarding claim 2, Ono et al. disclose the method comprising all of the limitation as of claim 1, wherein data is stored in the charge storing layer through a tunnel oxide layer, a charge storing nitride layer, and a blocking oxide layer stacked in sequence (floating gate tunnel oxide type memory cell; also as disclosed in prior figure 1).

Regarding claim 3, Ono et al. disclose the method comprising all of the limitation as of claim 1, wherein the first conductive type is P-type (p-type substrate), and the second conductive type is N-type (n-type drain/source region; see figures 5-6).

Regarding claim 4, Ono et al. disclose the method comprising all of the limitation as of claim 1, wherein the bulk voltage is about 0V (VB = 0 volt or ground).

Regarding claim 5, Ono et al. disclose the method comprising all of the limitation as of claim 1, wherein the voltage of the first electrical signal is switched between a first voltage and a second voltage at least one time, during the predetermined erase time, wherein the first and second voltages are greater than the gate voltage (at starting the process of the erasure, the source/drain voltage is at the programming voltage, then the two voltages are being switched, known as reverse biasing, therefore, the source and drain voltages are being switched).

Regarding claim 6, as best understood, Ono et al. disclose the method comprising all of the limitation as of claim 5, wherein the second electrical signal is substantially equal to the first and second voltages when the first electrical signal is substantially equal to the second and the first voltages, respectively, for the predetermined erase time (the second voltage is being switched (reversed bias) as of first voltage).

Regarding claim 7, Ono et al. disclose the method comprising all of the limitation as of claim 6, wherein the first voltage ranges from about 2V to about 6V, and the second voltage is about 10V (first is about 2 volts and second is about 14 is well in the range as claimed).

Regarding claim 8, Ono et al. disclose the method comprising all of the limitation as of claim 6, wherein both the gate voltage and the bulk voltage are about 0V (Vg = VB = 0 volt or ground).

Claims 9-13 and 14-16 contain the similar limitation as previously discussed in claims 1-8. Therefore, they are analyzed as previously discussed with respect to claims 1-8.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gene N Auduong whose telephone number is (703) 305-1343.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (703) 308-4910. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

GA
April 28, 2003

Gene N Auduong
Examiner
Art Unit 2818